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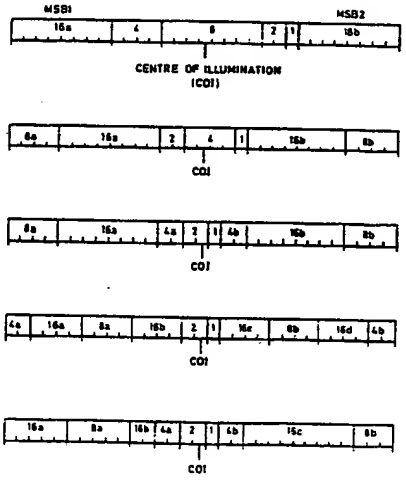

(57) Abstract

A display device includes a deformable mirror device (103, 105, 107) wherein grey scales are displayed using a time division modulation process f r switching each mirror device (M) within the display between an "on" state in which light is directed nto a display (101) and an "off" state in which light is n t directed nto the display (101). Each field period of the display system is divided into sufficient time intervals to allow grouping of the time intervals in which each mirror device (M) is switched t either the " n" state or the "off" state. This increases the temporal balance f the light from each mirror device (M) during each frame period of the display system and/or between consecutive frame periods.

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DISPLAY DEVICE

This invention relates to display devices. In particular the invention relates to display devices including an array of switchable elements, each switchable element being switchable between at least two states, the form of the image displayed by the display device being dependent on which state each switchable element is in.

Such switchable elements may take the form of light modulators which control the passage of light from a light source to the displayed image. Examples of light modulators include deflectable mirror devices as for example described in "Deformable Mirror Spatial Light Modulators" by Hornbeck, published in the Proceedings of SPIE, Vol. 1150, August 1989. Such deflectable or "deformable" mirror display devices include an array of deflectable mirror devices, each mirror device being mounted on a torsion element over a control electrode. Applying an electric field between each mirror device and the electrode causes the mirror device to pivot, thus changing the direction of light reflected from the mirror device.

Another example of a light modulator is a liquid crystal device.

Alternatively, the array of switchable elements may take the form of an array of light sources which themselves can be switched either on or off, for example, an array of light emitting diodes.

Generally such display devices are digital devices, that is each switchable element of the device is effective to switch the light passing from the element to the displayed image either "on" or "off" so as to produce either "white" or "black" pixels on the displayed image. It is, however, possible to display grey scale images by controlling the time for which each switchable element of the device is in a state such that light from the element arrives at the displayed image, and using the integrating response of the human eye of an observer who will perceive a grey scale image from the element.

An example of such an arrangement is described in GB 2014822 which discloses a display device incorporating an X-Y array of energizable light emitting devices. The display device described in GB

2014822 takes data in binary digital forms, for example via an 8 bit signal, the device being driven a line at a time in a number of periods during which the modulators may be "on" or "off". The "on"/"off" state of each pixel during each time period is determined by the state of the corresponding bit of the digital input data.

Display devices incorporating light modulators in the form of deformable mirror devices operate in an analogous manner. In deformable mirror devices, however, the entire pixel array is driven simultaneously in sympathy with the video source vertical scan rate.

The eight time periods within each display frame period are of different lengths. The length of the time period corresponding to the least significant bit (LSB) in the input signal for any particular frame is set at a predetermined value, the duration of the time period corresponding to the next to the least significant bit being twice as long as that corresponding to the least significant bit, and so on. Thus, the length of the time period corresponding to the most significant bit (MSB) for such an eight bit

input signal is 128 times that corresponding to the least significant bit (LSB). Provided that all the time periods are included within a display frame period of less than around 20 msecs duration, the human eye will integrate the periods and respond as if to a single period having a level of brightness corresponding to the binary signal value. At the end of each sub-frame period corresponding to a single bit of the input signal, a resetting signal is supplied to all the elements of the array in order to switch the elements into a rest position in some systems, or into the state determined by the next bit signal.

Such display systems, using time division multiplex addressing of the switching elements at least partially to display grey scales, are used in large screen projectors. It is found however that where such large screen projectors are used to display motion video signals, there are formed bands of twinkling pixels at certain mid-grey brightness levels. Furthermore, for the same mid-grey brightness levels, the displayed image can break up into "chunky" pixels if a viewer blinks his eyes, moves his head, or waves his fingers in front of his eyes or in front of the

projection lens. These effects are sometimes known as "dynamic contouring".

It is an object of the present invention to provide a display system incorporating an array of switchable elements wherein these problems are at least alleviated.

According to a first aspect of the present invention, there is provided a display system including an array of switchable elements wherein grey scales are at least partially displayed using a time division modulation process for switching each element between an "on" state in which light is directed onto a display, and an "off" state in which light is not directed onto the display, wherein each frame period of the display system is divided into sufficient of the time intervals in which each element is switched to the "on" or "off" state in order to increase the temporal balance of the light from each element.

The invention thus arises in the appreciation by the inventors that the effects defined above as "dynamic contouring" can be reduced by manipulation of the time division multiplex addressing scheme.

Thus, according to a second aspect of the present invention, a display system including an array of switchable light directing elements includes means for modifying the times for which each element directs light onto a display so as to reduce adverse effects caused by the temporal addressing of the switchable elements.

A number of embodiments of a display system in accordance with the invention will now be described by way of example only with reference to the accompanying figures in which:-

Figure 1 is a schematic diagram of an overview of a display system of known form;

Figure 2 is a schematic diagram of a spatial light modulator array incorporated in the system of Figure 1;

Figure 3 illustrates the illumination of a mirror device in the array of Figure 2;

Figures 4a-4e illustrate five examples of a known time division multiplex address scheme for achieving grey scales in the system of Figure 1;

Figure 5 illustrates an example of a known time division multiplex address scheme for two adjacent mirror devices in the arrays incorporated in the display system of Figure 1;

Figures 6a-6e illustrate five examples of a modified time division multiplex address scheme used in a display system in accordance with an embodiment of the invention;

Figure 7 illustrates a first example of a bit weight distribution scheme for use in a display system in accordance with an embodiment of the invention;

Figures 8a-8d illustrates an example of a computer simulation of the light output from a single pixel resulting from a prior art display system;

Figures 9a-9d illustrates an example of a computer simulation of the light output from a single

pixel resulting from a modified display system in accordance with an embodiment of the invention;

Figure 10 illustrates a second example of a bit weight distribution scheme for use in a display system in accordance with an embodiment of the invention;

Figure 11 illustrates a third example of a bit weight distribution scheme for use in a display system in accordance with an embodiment of the invention;

Figure 12 illustrates a fourth example of a bit weight distribution scheme for use in a display system in accordance with an embodiment of the invention;

Figure 13 illustrates a modification of the bit weight distribution scheme of Figure 12.

Figure 14 illustrates part of the display system designed to implement a modified addressing system in accordance with an embodiment of the invention.

Figure 15 illustrates the sequencer incorporated in the apparatus of Figure 14; and

Figure 16 illustrates the contents of the frame store incorporated in the apparatus of Figure 14.

Referring firstly to Figure 1, the particular example of a display system to be described is arranged to project a colour image onto a display screen 101. The display system includes a light source 103 which may take any suitable form, for example an arc lamp. The light source 103 is arranged such that the beam from the source is directed onto three planar deflectable mirror display devices 105,107,109 as will now be described.

Positioned in the light path between the light source 103 and the first deflectable mirror device 105 are two dichroic mirrors 111,113. The first dichroic mirror 111 is designed and angled to reflect blue light onto the second planar deflectable mirror display device 107 and transmit all other incident light. The second dichroic mirror 113 is designed and angled so as to reflect red light onto the third planar deflectable mirror device 109 and transmit the remaining green component of the light from the source 103 onto the first deflectable mirror display device 105.

The three deflectable mirror devices 105,107,109 are arranged to be capable of reflecting the three colour components of the beam from the source 103 so as to direct the spatially modulated beam through a projection lens 115 onto the display screen 101.

Referring now also to Figures 2 and 3, each deflectable mirror device (DMD) 105,107,109 comprises an array of m x n deflectable mirror devices, typically 768 x 576 mirror devices for a low resolution display system or 2048 x 1152 mirror devices for a high resolution display system. Each array 117 is connected to a driver circuit 119 which receives an electronic colour video signal from the control circuit indicated generally as 121, and addresses each of the mirror devices M_{11}-M_{mn} as, for example, described in the applicant's earlier International Patent Application, PCT/GB92/00002 dated 4th January 1992 (incorporated herein by reference). Dependent on the applied address signal, each mirror device M is caused to take one of two different positions corresponding to an "on" state in which the reflected light is directed in a first path 123 and an "off" state in which the reflected light is directed in a second path 125. The second

path 125 is chosen such that light reflected along this direction is directed away from the optical axis of the display system and thus does not pass into the projection lens 115.

Thus, each DMD array 117 is capable of representing a two dimensional image, those mirror devices M which are tilted to the "on" state appearing bright and those which are tilted to the "off" state appearing dark. By varying the ratio of the "on" period to "off" period, that is by a temporal modulation technique, grey scale can be achieved as will be described in more detail hereafter.

Turning now particularly to Figure 3 the angle through which each mirror device M is deflected between the "on" state and the "off" state is relatively small. Thus in order to achieve good discrimination between the "on" and "off" states the incident light beam 127 from the source 103 is directed towards each spatial light modulator 105,107,109 at an angle measured from the normal to each device of around 20^{o}.

When an individual mirror device M is lying parallel to the plane of the array 117, the incident beam 127 is reflected at a corresponding angle of 20^{o} to the normal along an "off" path 122 into a beam dump (not shown). When the control signal from the driver circuit 119 sets the mirror device M into a first deflection state at a first angle to the plane of the array 117, the incident beam 127 is reflected along the direction 125 in a further "off" path into the beam dump. When the control signal from the addressing circuit 119 sets the mirror device M into a second deflection state at a second angle to the plane of the array 117, the incident beam 127 is reflected out along the normal to the array along the "on" path 123.

Referring now to Figures 4a-4e, these Figures illustrate the time division multiplex address sequence of each of the mirror devices M of the DMD array 117 which enables grey scales to be displayed on the screen 101. For the sake of simplicity, the example shown in Figures 4a-4e corresponds to a five bit input video signal. Thus each Figure 4a-4c represents a time frame of a particular mirror device M which is divided into

thirty-one equal time intervals, the horizontal direction thus representing a time axis.

Figure 4a corresponds to the situation where the mirror device M is arranged such that maximum brightness is displayed on the display screen 101 for the duration of a frame period of the display device. Thus, the mirror device M is switched to the "on" state for a duration of sixteen time units (corresponding to the MSB), eight time units, four time units, two time units, and finally one time unit, (corresponding to the LSB). Thus the integrated brightness level for the particular mirror device M in array 117 is thirty-one units.

This can be contrasted with the situation shown in Figure 4b in which the mirror device M is switched to the "on" state only for the duration of the time period corresponding to the MSB during a single frame period of the display device. Thus, the integrated brightness of the mirror device M for the frame period is sixteen units.

Similarly Figure 4c illustrates the situation where the mirror device M is switched to the "off" state for the time interval corresponding to the MSB, and switched to the "on" state for the rest of the frame period. Thus, the integrated brightness of the mirror device M for the frame period is fifteen units.

Turning now to Figure 4d, this Figure illustrates two consecutive frame periods for a single mirror device M, and thus is to a different time scale from Figures 4a-4c. In this particular example, the sequence illustrated in Figure 4b is followed by the sequence illustrated in 4c. Thus, in the example shown in Figure 4d, the second half of the first frame period and the first half of the second frame period are both dark corresponding to an "off" state of mirror device M. This results in a time interval of one frame period when no light appears on the display screen 101 for the pixel corresponding to mirror device M. It has been appreciated by the inventors that this will manifest itself as a dark flash on the display screen 101 which will be discernible to an observer.

The situation illustrated in Figure 4e also shows two consecutive frame periods for a single mirror device M, and is thus shown with the same horizontal time scale as that of Figure 4d but with a reversed frame sequence. In this particular example there is a total frame period consisting of the second half of the first frame period and the first half of the second frame period when the display screen is continuously illuminated. It has been appreciated by the inventors that this will appear to an observer as a white flash on the display screen 101.

If the drive signal to the mirror device M fluctuates between the bit sequences of Figure 4d and 4e due to, for example, video quantisation noise, then that pixel will appear to twinkle in sympathy with the noise, that is the phenomenon known as "dynamic contouring". Thus, it has been appreciated by the inventors that at certain mid-grey brightness levels, situations of the type illustrated in Figures 4d and 4e will give rise to twinkling pixels in the projected image on the screen 101. Furthermore, this video noise will also result in quantisation time jitter of the critical bit transitions within the analogue to digital converter used to process the video input signal such

that the twinkling pixels spread over a distinct band.

It has also been appreciated by the inventors that the situations depicted in Figures 4d and 4e can also give rise to apparent "dynamic contouring" of the image when an observer blinks his eyes, moves his head, or waves his fingers in front of his eyes or in front of the projection lens 105. This can be seen with reference to Figure 5 which illustrates a single frame time period for each of two adjacent mirror devices M_{11} and M_{12}, the horizontal scale thus being different to that of Figure 4a-e. The first mirror device M_{11} is arranged such that the MSB only is "on", all the other bits being off. In the second mirror device M_{12}, the MSB is "off" with all the other bits being "on". Thus, it will be seen that the image pixel formed from the light from M_{11} will arrive on the display screen 107 half a frame period before the image pixel formed from the light from M_{12}.

If the head of the observer is moving, or the observer's eyes scan across the projected image on the display screen 101, for example when following a moving object on the displayed image, the two pixels corresponding to the light from mirror devices M_{11} and M_{12} will appear to move relative to the background and hence relative to each other. This leads to the pixel corresponding to light from the "later" addressed mirror device M_{12} appearing to move in the opposite direction to the scanning direction of the observer's eyes, whilst the pixel corresponding to light from the earlier addressed mirror device M_{11} will appear to move in the same direction as the scanning direction of the observer's eyes. Thus, if the direction of movement of the observer's eyes is in the direction from the mirror device M_{11} to the mirror device M_{12}, the apparent displacement of the two pixels will cause the pixels to appear to overlap, leading to an apparent bright up of the displayed image at that point on the display screen 101.

Conversely, where the direction of movement of the observer's eyes is in the opposite direction, that is from the mirror device M_{12} to the mirror device M_{11}, the two pixels will appear to separate leading to an apparent darkening of the image at the corresponding point on the display screen 101. This effect will follow the pixels corresponding to major transitions in the displayed image much like contour lines on a map. Because these contour lines are not smooth, the apparent relative movement of the pixels will give the impression of a coarse pixel structure at these transition points to give an effect similar to that of inadequate display resolution.

Thus, it has been appreciated by the inventors that the bit transition "dynamic contouring" effects experienced in time division addressed optical modulators arise as a direct result of a temporal displacement of the bit pattern between adjacent display frames, or between adjacent pixels when the highest significant active bit turns "on" or "off". Furthermore, since the effect of the temporal shift between adjacent display frames is a unipolar fluctuation in light output, no matter how much

filtering is introduced by the observer's eye, the total disturbance energy cannot be reduced but only spread over a longer time interval.

The only way that this "dynamic contouring" due to bit transitions can be reduced is either to eliminate or to minimise such temporal shifts in the bit pattern at the critical bit transitions. This is difficult to achieve completely for time division multiplex addressed display systems as temporal displacements are intrinsic to their operation. However, the problems can be alleviated if the unipolar disturbance resulting from the temporal shift can be converted to a bipolar disturbance (as will be illustrated with reference to Figures 8 and 9), and by maximising the frequency and minimising the amplitude content of the disturbance (as will be illustrated with reference to Figures 10,11,12 and 13).

There now follow examples of modified time multiplex addressing schemes used in a display system in accordance with the invention, which have been designed in order to implement the elimination or minimisation of temporal shifts in order to alleviate

the problem of display flicker and "dynamic contouring".

Turning now to Figures 6a-6e these figures illustrate modified versions of the bit weight sequences illustrated in the prior art arrangements of Figures 4a-4d used in a display device in accordance with the invention.

Figure 6a illustrates the situation where only the MSB of 16 time units is split into two part sub-frames MSB1 and MSB2 each of 8 time units duration and labelled as 16a and 16b. A centre of illumination (COI) can be defined for the display frame period, this occuring at the centre of the frame period. A qualitative analysis of the benefit of the scheme can then be obtained by considering the "moments" of the various bit weights about the centre of illumination in analogy to dynamic balancing in a mechanical system. As both MSB1 and MSB2 will correspond to the particular mirror device M either being either "on" or "off", it will be seen that the individual moments will be equal in magnitude but opposite in sign. Thus, the contribution from these two part sub-frame periods to the moment of illumination will be zero. The second

longest sub-frame period, which is eight units long, is placed as close as possible to and symmetrically about the centre of the frame period in order to minimize its contribution to the moment of illumination. The remaining sub-frames of 4,2 and 1 are positioned as symmetrically as possible about the centre of illumination in order to minimise changes in the moment of illumination of the frame for the various possible combinations of seven units (4 + 2 + 1), eight units (single 8 sub-field), fifteen units (8 + 4 + 2 + 1), sixteen units (16a + 16b), twenty-three units (16a + 16b + 4 + 2 + 1), and twenty-four units (16a + 16b + 8).

Figure 6b shows a modification of the scheme of Figure 6a in which the second most significant bit sub-frame of eight units is also divided into two parts 8a and 8b, each of four units duration. If the centres of the part sub-frames 16a and 16b are separated by half a frame period as shown in Figure 6b, then at the sixteen unit mid brightness level, the flicker fundamental frequency component of the light output at the display frame rate is eliminated, and hence any perceived display flicker will be minimised.

Turning now to Figure 6c, in this bit weight distribution scheme the three most significant bits are each split into equal parts. Thus, the sixteen unit sub-frame, the eight unit sub-frame and the four unit sub-frame are all divided into parts 16a and 16b, 8a and 8b, and 4a and 4b respectively. As the part sub-frames 16a and 16b already have the optimum position as shown in Figure 6b, the part sub-frames 4a and 4b are placed adjacent to these part sub-frames, but towards the centre of the display frame period.

Turning now to the bit weight distribution scheme of Figure 6d, this scheme shows the MSB being split into four equal part sub-frames, each of four units duration, that is 16a,16b,16c and 16d. The next two most significant bits are each split equally into two part sub-frames 8a and 8b, and 4a and 4b respectively. In this particular scheme the MSB part sub-frames 16a,16b,16c and 16d are spaced by a quarter of a frame period. This not only removes the fundamental sixteen unit flicker component but the second harmonic as well. The part sub-frames 8a and 8b are placed half a display frame period apart such that the fundamental flicker components at the eight unit brightness level is also eliminated. This leaves two gaps at each end

of the frame period where the part sub-frames 4a and 4b fit in symmetrically.

Turning now to Figure 6e, this figure illustrates a bit weight distribution scheme in which unequal bit splitting is employed. In this scheme MSB is split into three part sub-frames , 16a of five units duration, 16b of two units duration and 16c of nine units duration. The next most significant bit is split into two part sub-frames 8a of five units duration and 8b of three units duration. The third most significant bit is split into two equal part sub-frames 4a and 4b each of two units. This figure thus illustrates a bit weight distribution scheme in which the sub-frames may be divided into an uneven number of part sub-frames of unequal duration, It can be shown, however, that the address scheme illustrated in Figure 6e does not give as good control of the centre of illumination as that shown in Figure 6d.

Referring now to Figure 7, this figure illustrates a bit weight distribution scheme in which the effect of flicker is minimised. As shown in this figure, the MSB is split into eight equal part sub-frames, the next MSB into four equal part

sub-frames, and the next MSB into two equal part sub-frames. Thus the maximum part sub-frame duration is now two units such that the display frame is divided into fourteen equal part sub-frames (A-G) of two units duration, one sub-frame of two units duration and one sub-frame of one unit duration to make a total of 31 units as before.

The left hand vertical column in Figure 7 represents increasing levels of display brightness during a single frame between the minimum of zero and the maximum of thirty one units. The presence of an X in a part sub-frame indicates that the corresponding mirror device M is switched to the "on" state at that particular time, lack of an X indicating an "off" state. The timing of the reset pulses for the mirror devices in the DMD array 117 is also shown in the figure, it being apparent from Figure 7 that reset pulses must be applied every two units to prepare the mirror devices M for their next orientation state.

The purpose of the scheme illustrated in Figure 7 is to spread the periods during which the mirror device M is "on" evenly throughout the frame period. However, since thirty-one is a prime number, the spreading can

never be perfect. It can be seen that for levels of illumination of 0-3 units and 28-31 units, even spreading of the illumination throughout the frame period does not occur. However, at these illumination levels, disturbance levels will be small and hence display artefacts will be much less apparent. For illumination levels 4 and 5, and 26 and 27, it can be seen that whilst the moment of illumination is greater, the fundamental disturbance frequency component has doubled to the second harmonic of the display cycle frequency. Similarly, for the other illumination levels, whilst the moment of illumination increases, so also does the fundamental light output disturbance frequency for each illumination level, this being shown by the figures in the right hand column of Figure 7.

It will be appreciated that by use of a bit weight distribution scheme as is shown in Figure 7, the one to one correlation between the video input signal and the address signals to the DMD array 117 has been removed other than for the LSB, and the next least significant bit. This can be accommodated by use of a suitable sequencer incorporating, for example, a ROM to effect the required bit conversion. Suitable apparatus will be described hereafter with reference to

Figures 14,15 and 16, Figure 7 effectively acting as a truth table for programming the ROM.

It will be seen that the scheme illustrated in Figure 7 is designed to reduce the effect of flicker caused by the effects of bit weight distribution within a single frame of the display system. Now, since the time division modulation information is received by the observer as a continuous stream, consideration must be given not only to the effects of bit weight distribution within a single display frame but also to the effects of moving from one display frame to the next. The effect of transitions between consecutive frames of the display system can be examined by computer simulation using a sliding window aperture function on the time division modulation serial data stream so as to simulate the integrating effect of the observer's eye. The variation in the mean value within the window, as the window moves along the bit sequence, will then be a measure of the light output disturbance as perceived by the observer. This will include flicker and other components in addition to the disturbances producing "dynamic contouring". Choosing a rectangular window aperture function of duration equal to the display frame period, whilst not fully

representing the behaviour of the eye, does, however, simulate with maximum clarity the "dynamic contouring" disturbances by only taking into account differences betwween adjacent display cycles.

Figures 8 and 9 illustrate the results of applying such a sliding window aperture function to the MSB and the next most significant bits i.e. MSB-1 bit transitions. Figure 8 shows the results for the bit sequence of Figures 4d and 4e, whilst Figure 9 shows the result of a modified bit sequence used in a display device in accordance with the invention. In Figures 8 and 9 the MSB is denoted by "M", the remaining LSBs are denoted by "L" and the MSB-1 is denoted by "H".

Consider in the first instance a sliding rectangular window sampling a sequence starting with the MSB and progressing to the LSB as shown in Figure 8a. When the light output increases by one LSB to turn all the LSBs "off" and the MSB "on", that is the situation illustrated in Figure 4e, it can be seen from Figure 8a that the resultant increase in light output from a given mirror device M is of a unipolar triangular form.

Similarly, for a decrease of one LSB as shown in Figure 8b, that is the situation illustrated in Figure 4d, the resulting decrease in light output is also of a unipolar triangular form.

Figure 8c illustrates the equivalent situation for the MSB-1 bit transition when an increase of one LSB turns all the LSBs "off" and the MSB-1 "on", the MSB being permanently "off". The disturbance in light output is also of a unipolar triangular form giving an increase in light output for the up transition.

Figure 8d illustrates the corresponding situation for 8d illustrates the corresponding situation for a decrease of one LSB showing the corresponding unipolar triangular decrease in light output.

Thus, from Figures 8a-8d it can be seen that for a given bit transition, the resultant disturbance in light output is of unipolar triangular form, the amplitude and duration of the disturbance increasing in proportion to the highest significance bit change transition between each pair of consecutive frames. It can also be seen that the disturbance peak amplitude is equal to the weight of the highest significance bit

change, and that the duration of the disturbance is twice the bit display interval for the same significance bit.

Figures 9a-9d illustrate the effects of bit splitting on the bit sequences of Figures 8a-8d when the part sub-frames of the split bits are positioned symmetrically about the centre of the display frame in a display system in accordance with the invention. Figures 9a and 9b show that in the case of MSB splitting, the unipolar disturbances of Figures 8a and 8b have been converted to a bipolar disturbance with the disturbance peak amplitudes halved, and the phase of the disturbance cycles reversing between the up and down transitions. The durations of the disturbances are, however, unchanged from that of Figure 8a.

Similarly, Figures 9c and 9d show that in the case of the MSB-1 transition, the unipolar disturbances of Figures 8c and 8d are converted to a single cycle bipolar disturbances of half the peak amplitude, with a phase reversal between up and down transitions. Again, the disturbance durations are unchanged.

It can be shown that splitting the bit display intervals still further reduces both the amplitude of the disturbances and the duration of the disturbances. In general, for a given highest significant bit change, the disturbance peak amplitude is given by (bit weight)/N, and the duration of the disturbance is given by (2*bit interval)/N where N is the bit splitting factor. Whilst, in principle, odd values of N can be employed, distributing the resultant part sub-frames poses additional problems. Furthermore, whilst is it not essential, implementation can be simplified by restricting N to binary multiples.

Defining the disturbance energy as the area under the disturbance waveforms of Figures 8 and 9, it can be shown by applying the sliding window technique used to generate Figures 8 and 9, that for minimum energy, the bit sequence must have any non-split bits in the centre of the display frame, and that the display frame should start and end with the split MSB intervals. Also, the significance of the split bits must decrease uniformly towards the centre of the display cycle. It can also be shown that placing the highest significance non-split bit at the centre of the display cycle results in that bit behaving as though it had been

split, but at the expense of the next lowest significance bit having a higher disturbance energy.

Disturbance energy considerations indicate that it is only the top four or five most significant bit weights that give rise to observable bit transition contouring on the displayed image. This is illustrated in Figure 10 for simple bit splitting having a maximum splitting factor N of two, and for which the LSB may be considered as all the remaining unsplit bit weights with the highest order unsplit bit located at the centre of the display frame.

Generally, the light output change between adjacent frames for a single mirror device M or between two adjacent mirror devices can be any value from zero to peak white. Obviously, for changes of zero illumination or the maximum peak white illumination, contouring is not a problem since it either does not occur or is totally masked by the step brightness change. However, a step change of a single LSB resulting in an MSB change can have a pronounced dynamic contouring effect.

Ideally but not necessarily, because of the random variation of step brightness changes in a real image, the allocation of the individual bit intervals within the display cycle should be carried out on a dynamic basis so as to minimise the amount of "dynamic contouring" generated by changes in illumination level between adjacent time frames. This dynamic allocation will need to take into account such factors as the highest significance bit change, change step size, and permissible degree of bit splitting.

It has been shown with reference to Figures 8 and 9, that the effects of contouring due to a single LSB step change in brightness decrease with decreasing highest significance bit change. It will be appreciated, however, that the "dynamic contouring" annoyance level is strongly influenced by the total number of bits changing, the degree of bit splitting, and by how these bits are distributed within the display cycle, all these factors affecting both the amplitude and frequency of the disturbances.

Defining a "dynamic contouring annoyance factor" as the product of the peak disturbance amplitude and the disturbance duration, then the absolute "dynamic

contouring" disturbance will vary as the square of the highest significance bit weight change. However, expressed as a fraction of the mean light output, the contouring disturbance will only vary in proportion to the highest significance bit weight change. Thus only the higher order bits should require splitting in order to reduce "dynamic contouring" effects.

In the case of changes in light output of greater than one LSB steps, the masking effect of the change on "dynamic contouring" will increase with increasing step size. Generally peak contouring disturbance amplitudes up to at least the change step size will be masked by the step change in light output. This masking effect will be further increased by reduction in the "contouring annoyance factor" brought about by bit splitting.

As explained above, the peak disturbance amplitude for a sliding window aperture equal to the display cycle period is proportional to the bit weight divided by the bit splitting factor N, then the effects of "dynamic contouring" will be masked for step brightness changes of this level or greater. The higher the bit splitting factor, the lower will be the

The MSB transition fundamental frequency component can be virtually eliminated by the dynamic bit splitting scheme illustrated in Figure 13 in which dynamic sub-frame allocation has some further optimisation, but at the expense of a small increase in disturbance energy for step changes in brightness greater than one LSB.

In Figures 12 and 13, the peak disturbance amplitude equals the step amplitude for step changes of greater than three LSBs. This could only be reduced further by a higher level of bit splitting although this will result in a corresponding increase in the amount of data which must be loaded into the DMD array 117. The schemes of Figures 12 and 13 require a total of fourteen bit display intervals for the top three MSBs plus 1+R intervals for the LSBs where R is the number of remaining LSBs.

Thus comparing Figure 7 with Figures 10 to 13, it can be seen that the distribution of the part sub-frames can be organised either for minimum steady state perceived display flicker as shown in Figure 7, or for minimum bit transition "dynamic contouring" due to bit transition disturbance as shown in Figures 10 to

13. Unfortunately, for many bit pattern combinations, minimum flicker and minimum "dynamic contouring" do not necessarily go together, though in general bit weight distributions that give minimum "dynamic contouring" do also give useful improvements in flicker performance even though these may not be optimum. Experience shows, however, that "dynamic contouring" artefacts are generally more objectionable than flicker, as apparent flicker is generally at extremely low levels.

Referring now to Figures 14, 15 and 16, these figures illustrate an example of addressing circuitry for implementing modified addressing schemes in accordance with the invention. Referring firstly particularly to Figure 14, the video input signal, which consists of one of three separate video signals representing the red, green and blue colour components of the image to be displayed, is applied to an analogue to digital converter (ADC) unit 129 together with a synchronising signal. The output of the ADC unit 129 is applied to a gamma correction unit 131 to remove the gamma correction signal which is normally present in video signals for display on a cathode ray tube.

The output of the gamma correction unit 131 is applied to a data formatting unit 133 to convert the word serial video input into a form suitable for addressing the DMD array 117. The data formatting unit 133 is arranged to address alternately two frame stores 135, of which only one is illustrated in Figure 8. Each frame store 135 is arranged to store the video data for each element M of the DMD array 117, and to supply this data to each element M within the DMD array 117 via the driver circuit 119. The form of the frame stores 135 will be described in more detail hereafter.

A sequencer 137, whose form will be described in more detail hereafter, is arranged to supply the reset signals to the mirror devices in the DMD array 117 at the end of each bit frame display interval so as to enable all the mirror devices M to assume a 'rest' orientation as illustrated in Figure 3 prior to being deflected into their next required orientation relative to the illuminating beam. Whilst one frame store 135 is supplying data to the DMD array 117, the other frame store 135 is receiving fresh video data from the data formatting unit 133.

Turning now particularly to Figure 15, the sequencer 137 includes a read only memory (ROM) 139 programmed with the display time lengths of each bit field. The ROM 139 is addressed by a programmable counter 141 which is clocked by the output of a second programmable counter 143 which is, in turn, clocked by clock pulses from a clock 145. Counter 143 is programmed such that the total number of counts produced within each frame time is determined by a preset value obtained from the ROM 139. The count cycle of counter 143 thus defines the display time duration for the current bit weight, whilst counter 141 cycles through each bit display interval making up a complete display cycle. The output of counter 141 also defines the next bit weight to be transferred from the relevant frame store 135 to the DMD array 117.

At the end of each display interval, counter 143 generates an output signal which resets the DMD array 117 and transfers the new information to the mirror devices M, presets itself with next bit frame display time, and finally increments counter 141 to select the next bit weight.

Turning now particularly to Figure 16, and assuming an 8 bit video input signal, each frame store 135 includes 8 planes P1,P2...P8. Each plane holds data for DMD array 117 corresponding to a single bit weight of the input video signal. Thus, plane P1 corresponds to the MSB, plane P2 corresponds to the next most significant bit and so on up to P8 which corresponds to the LSB. The sequencer 137 provides appropriate control signals to each frame store 135 to write a single bit plane of data into the DMD array 117 ready for display during the next bit display interval. The net result is that each mirror device M of the DMD array is reset in a time multiplexed manner.

Implementation of bit display schemes in accordance with the invention, such as those shown in Figures 7,10,11,12 and 13 is achieved by suitable programming of the sequencer ROM 139, and setting the number of bits to suit the new sequence. The distribution of the input bit weights between the additional display intervals is achieved within the gamma corrector 131 by modifying the look-up table, which is generally incorporated within the gamma corrector, to increase the output bus width.

It will be appreciated that whilst the particular display device described herebefore by way of example relates to a display device including three deformable mirror devices, the invention is equally applicable to other forms of display device including other forms of light modulators such as liquid crystal devices and also display devices which incorporate an array of switchable light sources.

It will also be appreciated that whilst in the particular embodiment described the grey scale is achieved totally by means of time division modulation of the switchable elements, the invention is also applicable to display systems in which part of the grey scale is achieved by binary modulation of the light source. Such a display system is described, for example, in the applicant's copending UK Patent Application No. GB 9223114.1 which is incorporated herein by reference.

It will also be appreciated that whilst the particular colour display system described herebefore by way of example incorporates three separate light modulators 105,107,109 one for each colour red, blue and green the modulators operating in parallel, the

invention is equally applicable to sequential colour display systems employing a colour wheel or similar device for changing the colour of the light in a controlled manner. In such a sequential colour system, the colours are displayed sequentially from a single light modulator such that light from each colour is temporarlly displaced by one third of a display frame period. Modulation temporal displacement of the light arriving at the display screen 101 will be in addition to the delays caused by the sequential colour projection. The "dynamic contouring" effect observed in prior art systems of this type will be analogous to those observed in a parallel colour system, but with colour artefacts in addition to brightness artefacts. It will be seen that an addressing scheme as described hereabove will reduce such artefacts. However, motion effects when observed in such a colour sequential system will be different from those observated in a parallel colour system, the one third of a frame period delays produced by colour sequential systems introducing colour fringing to moving objects. The worst case delay will, therefore , again be half a frame period, this resulting in a similar effect to that seen in prior art parallel colour systems. Thus, display systems in accordance with the invention using,

for example, an addressing system as described above can be used to alleviate this problem in sequential colour systems.

CLAIMS

1. A display system including an array of switchable elements wherein grey scales are at least partially displayed using a time division modulation process for switching each element between an "on" state in which light is directed onto a display, and an "off" state in which light is not directed onto a display, wherein each frame period of the display system is divided into sufficient time intervals so as to enable ordering of the time intervals in which each element is switched to the "on" or "off" state in order to increase the temporal balance of the light directed from each element, and the display system includes means for effecting said ordering.

2. A display system according to claim 1, in which the temporal balance of the light directed from each element is increased during each frame period of the display system.

3. A display system according to either of the preceding claims, in which the temporal balance of the light directed from each element for the transitions between adjacent display frame periods is increased.

4. A display system according to any one of the preceding claims, wherein each frame period is divided into a number of sub-frame periods of different lengths corresponding to periods in which each element is switched "on" or "off", and at least one of the sub-frame periods is divided into at least two part sub-frame periods.

5. A display system according to claim 4, in which said one sub-frame period corresponds to the longest sub-frame period.

6. A display system according to claim 4, in which the part sub-frames are dynamically balanced in each display frame period.

7. A display system according to any one of claims 4 to 6 when dependent on claim 3, in which the position of each part sub-frame is positioned within the display frame period according to the size of the step brightness change of the light directed onto the display between the adjacent frame periods.

8. A display system according to any one of the preceding claims, wherein grey scales are partially displayed using a modulated light source which is switched synchronously with the switching of the switchable elements.

9. A display system according to any one of claims 4 to 8, in which each frame period is divided into said sub-frames in a binary manner.

10. A display system according to any one of the preceding claims, in which the array of switchable elements is a deflectable mirror device.

11. A display system according to any one of the preceding claims, in which the display system is a parallel colour display system, each element being effective to direct light of one colour component.

12. A display system according to any one of the preceding claims in which the display system is a sequential colour display system, each element being effective to direct light of different colour components sequentially.

13. An apparatus substantially as hereinbefore described with reference to Figures 6 and 7, and 9-16 of the accompanying Figures.

14. A method of addressing an array of switchable elements of a display system, wherein grey scales are at least partially displayed using a time division modulation process for switching each element between an "on" state in which light is directed onto a display, and an "off" state in which light is not directed onto the display, comprising dividing each frame period of the display system into sufficient time intervals so as to enable ordering of the time intervals in which each element is switched to the "on" or "off" state in order to increase the temporal balance of the light directed from each element, and causing said ordering.

15. A method according to claim 14, in which the temporal balance of the light directed from each element is increased during each frame period of the display.

16. A method according to claim 14 or claim 15, in which the temporal balance of the light directed from each element for the transition between the adjacent display frame periods is increased.

17. A method of addressing an array of switchable elements substantially as hereinbefore described with reference to Figures 6 and 7, and 9-16 of the accompanying Figures.

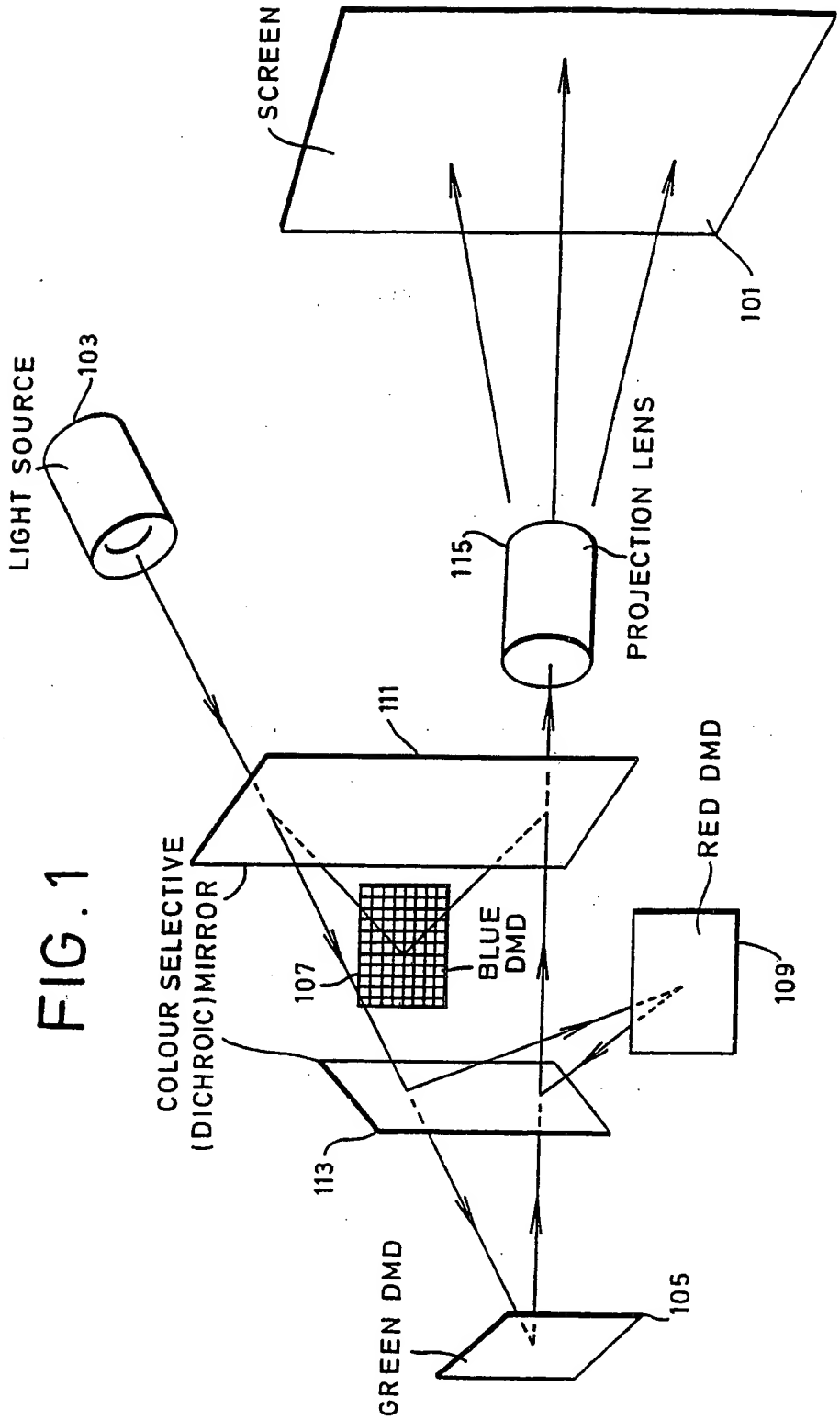

SCREEN
101
LIGHT SOURCE
103
115
PROJECTION LENS
111
RED DMD
109
COLOUR SELECTIVE
(DICHROIC)MIRROR
BLUE
DMD
107
113
GREEN DMD
105

FIG. 1

FIG. 2

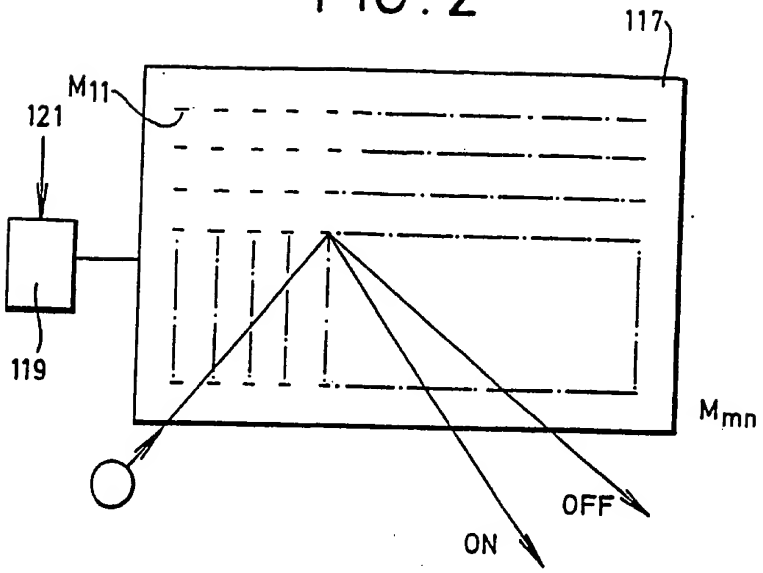


FIG. 3

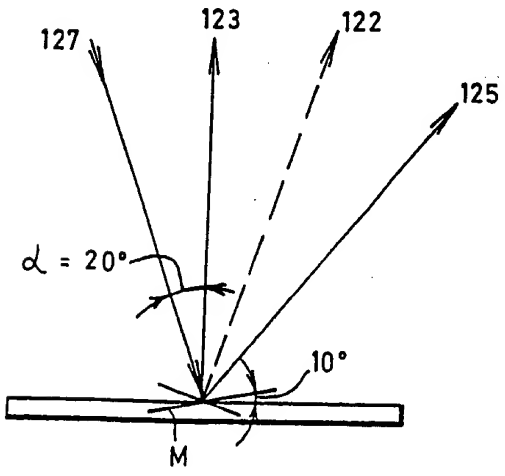


FIG.4a

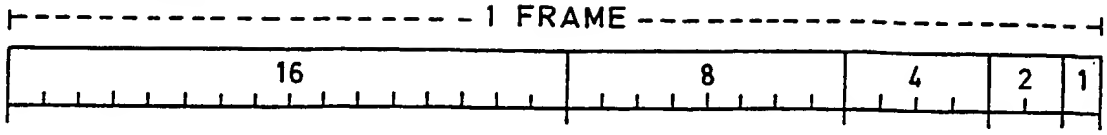


FIG.4b

FIG.4c

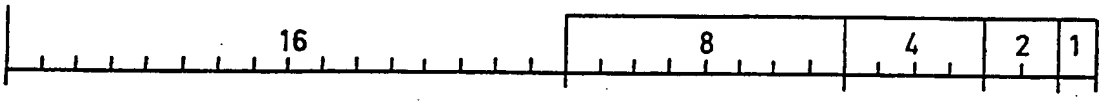


FIG.4d

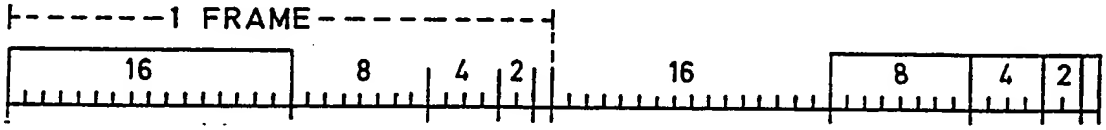


FIG.4e

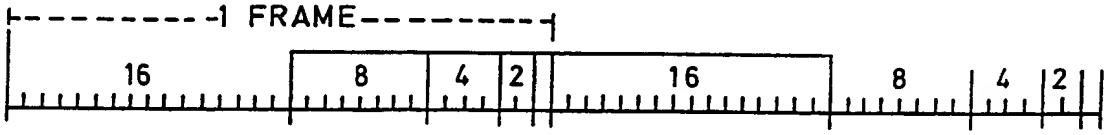


FIG.5

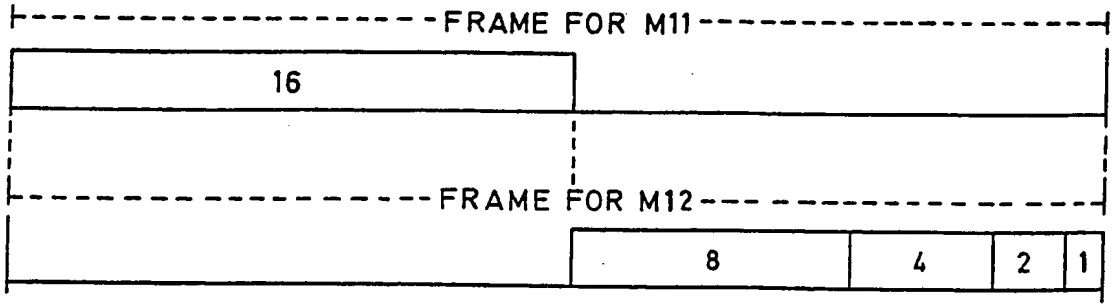


FIG.6a

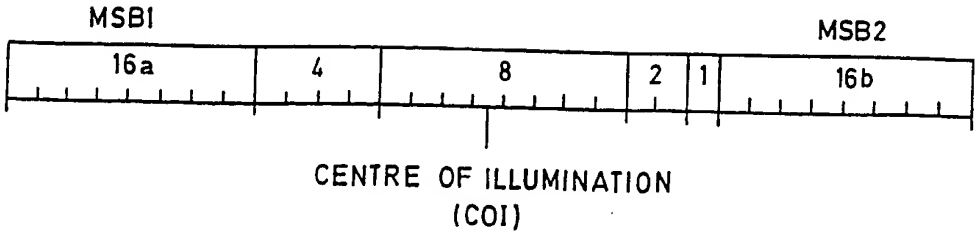


FIG.6b

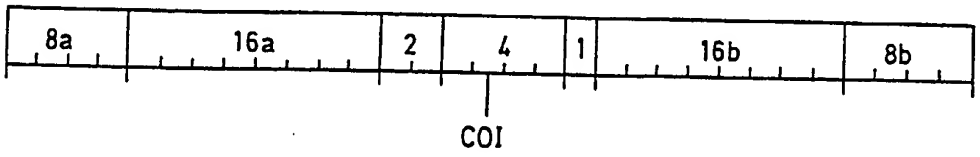


FIG.6c

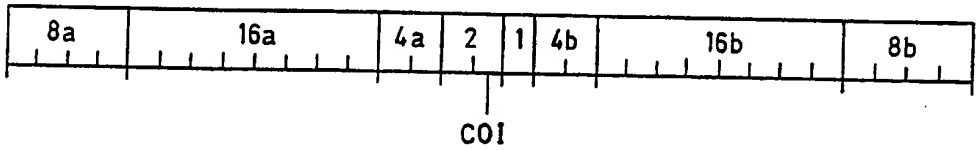


FIG.6d

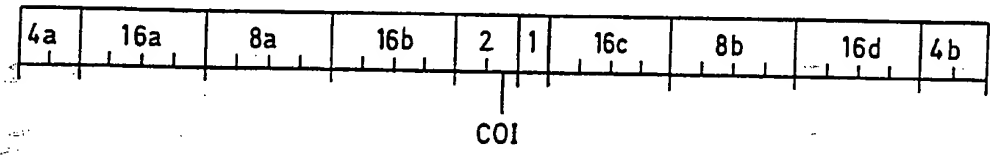
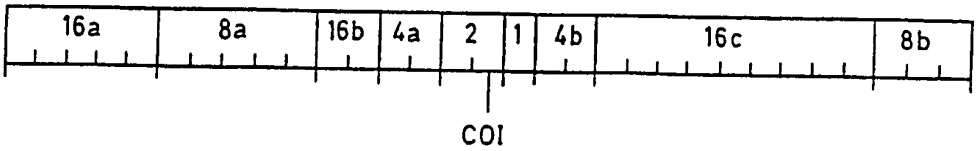
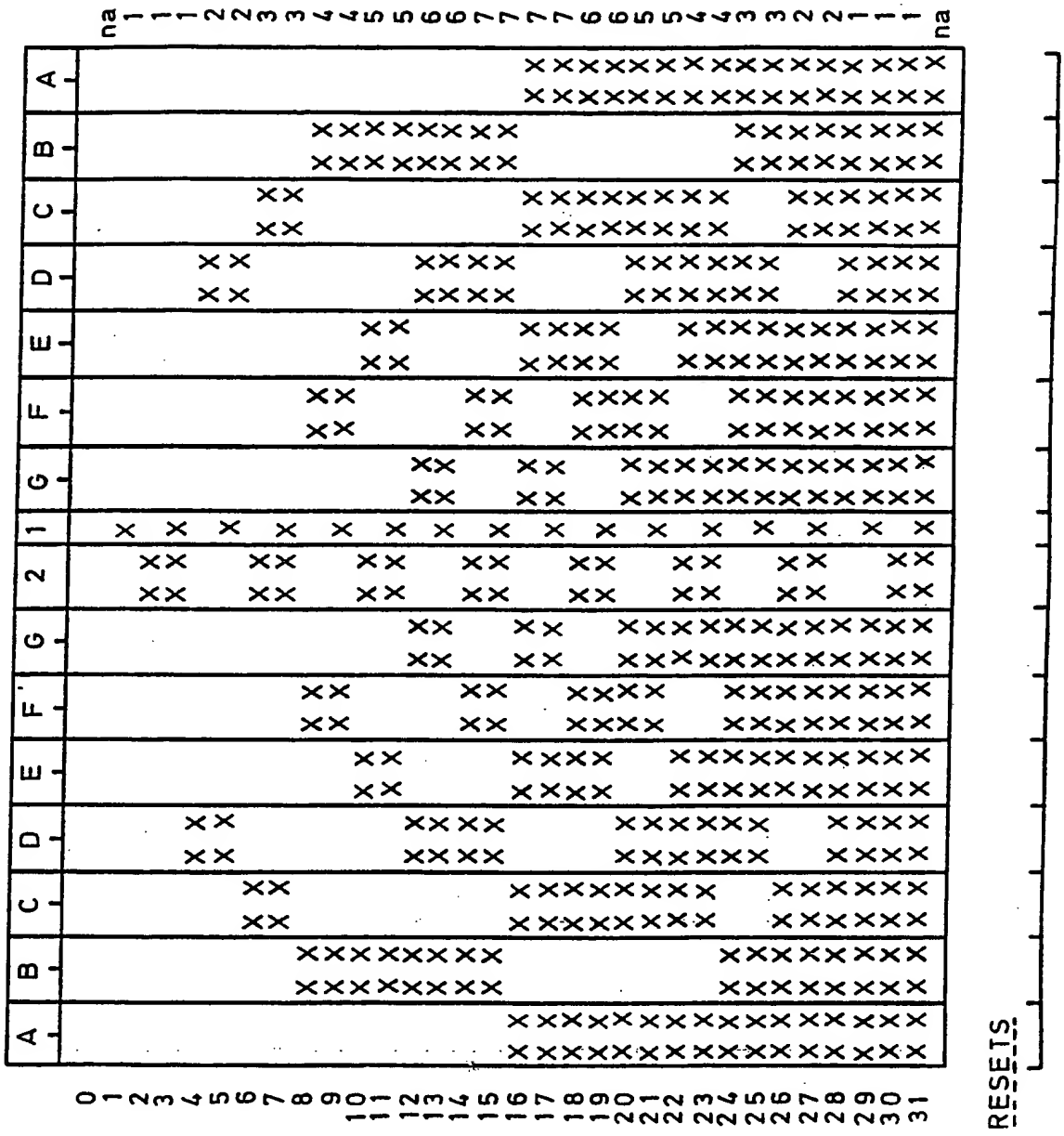


FIG.6e

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RESETS

FIG. 7

FIG.8a

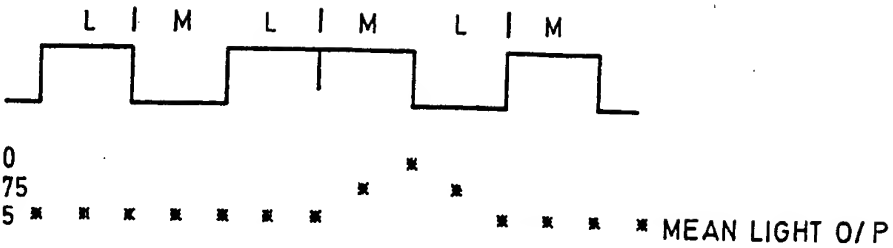


FIG.8b

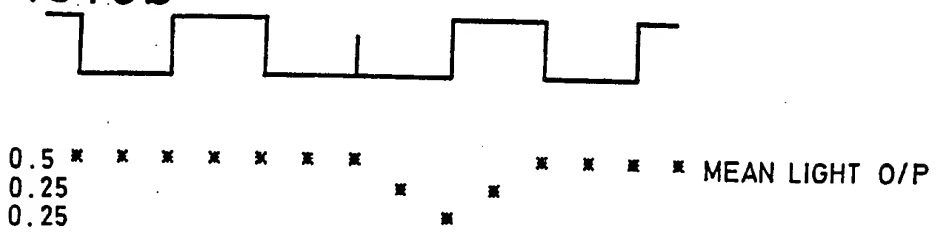


FIG.8c

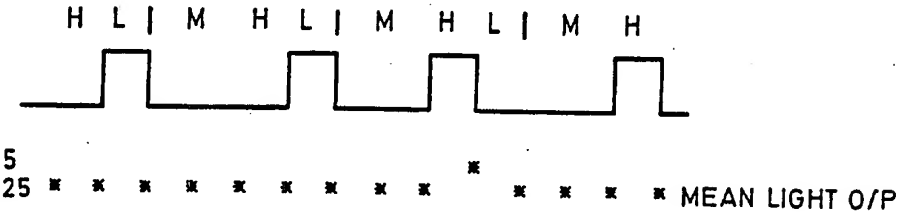


FIG.8d

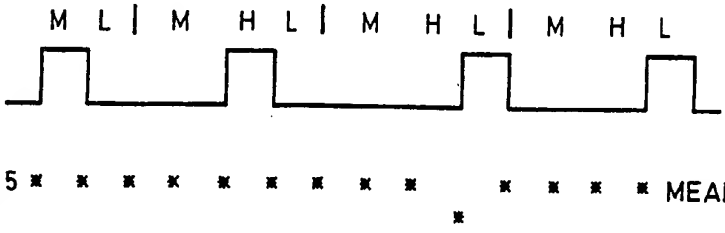


FIG. 9a

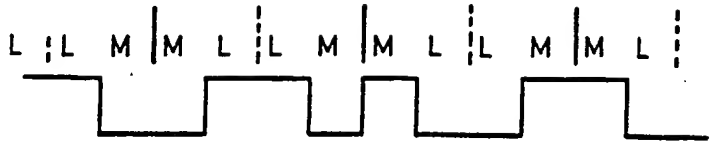


FIG. 9b

FIG. 9c

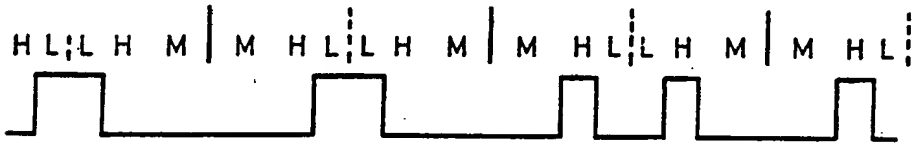
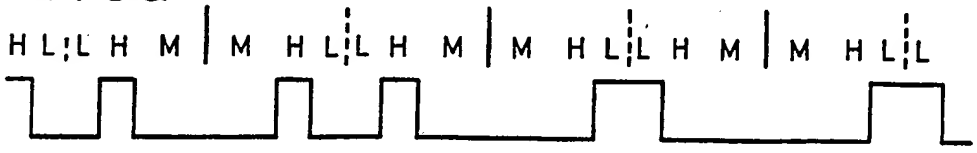
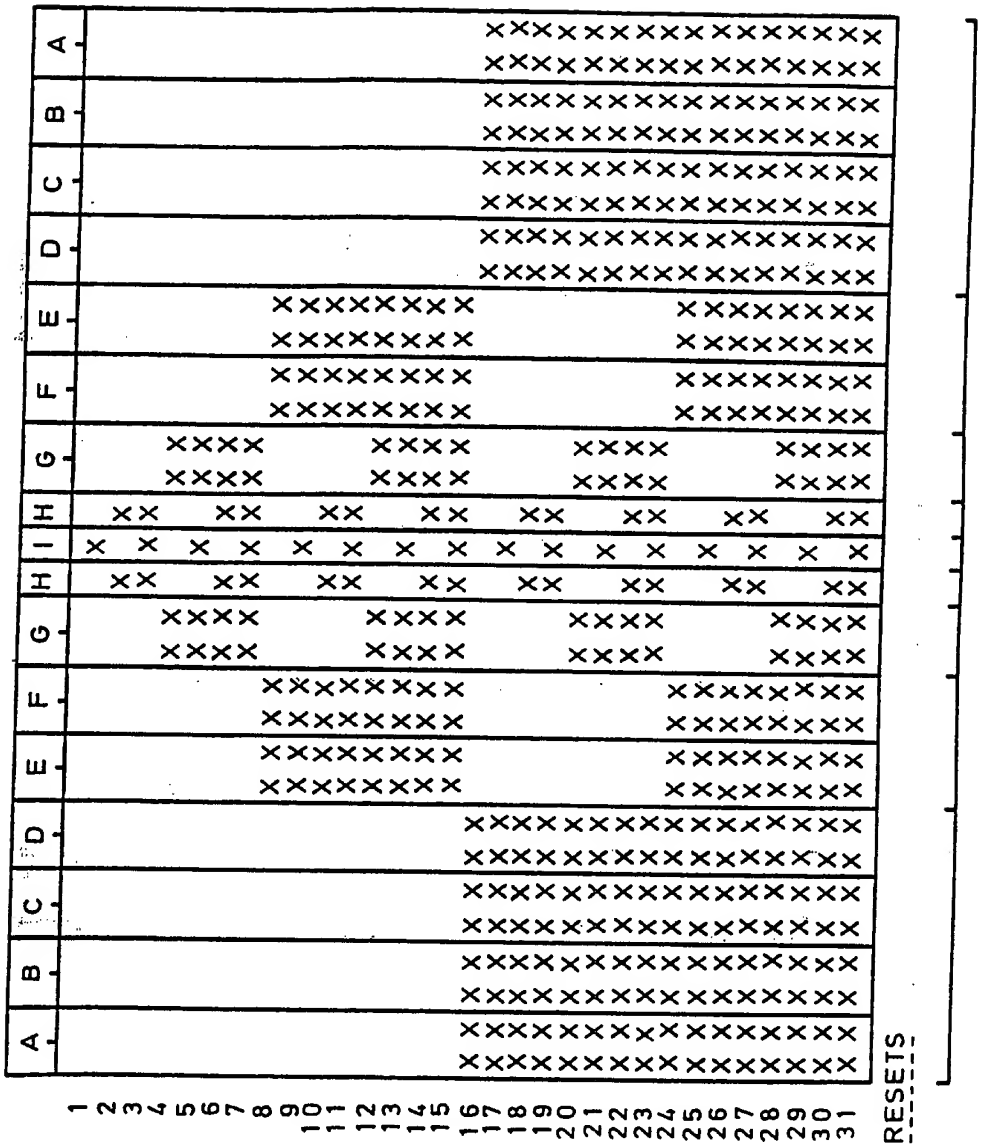


FIG. 9d

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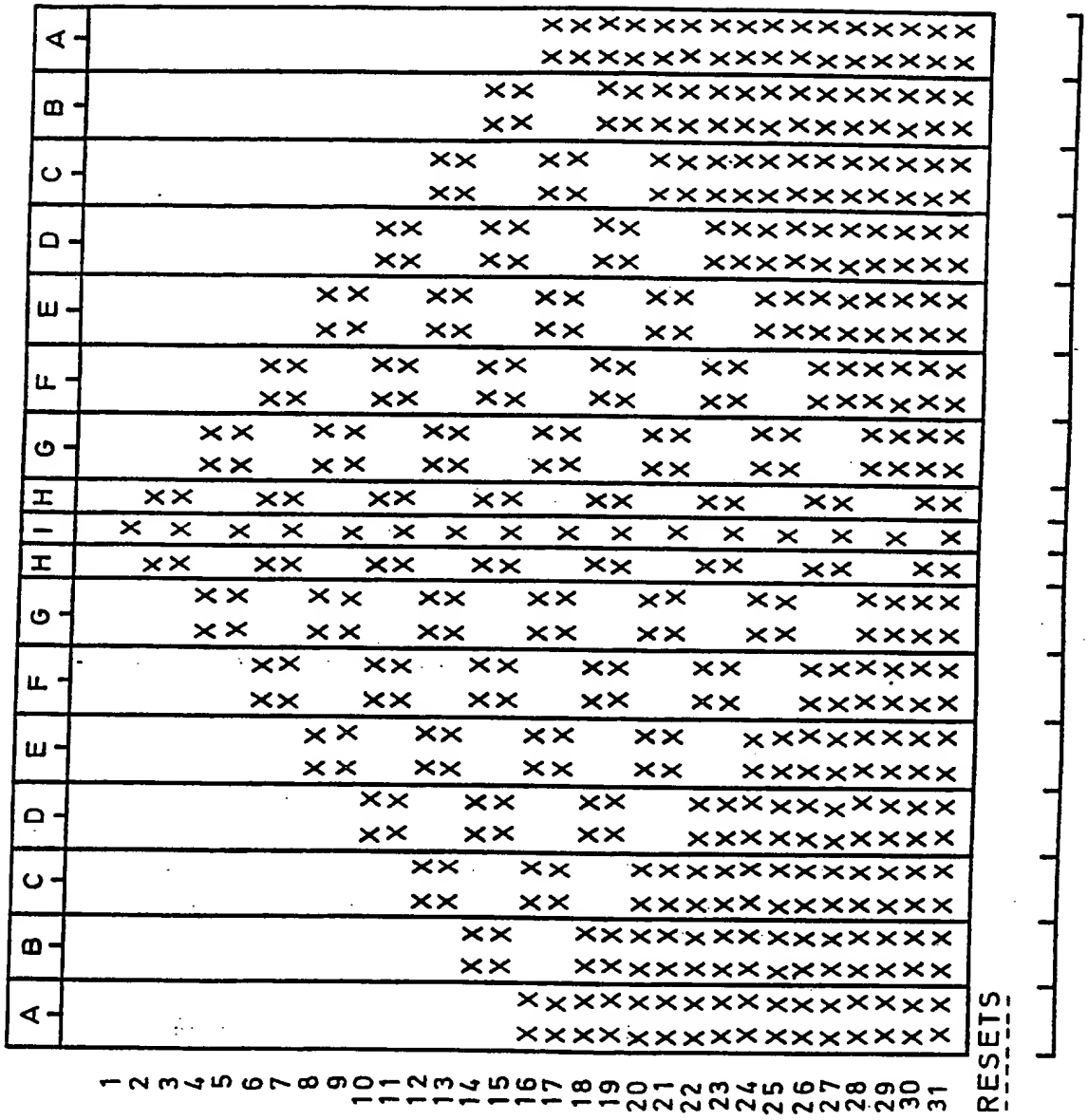
RESETS

FIG. 10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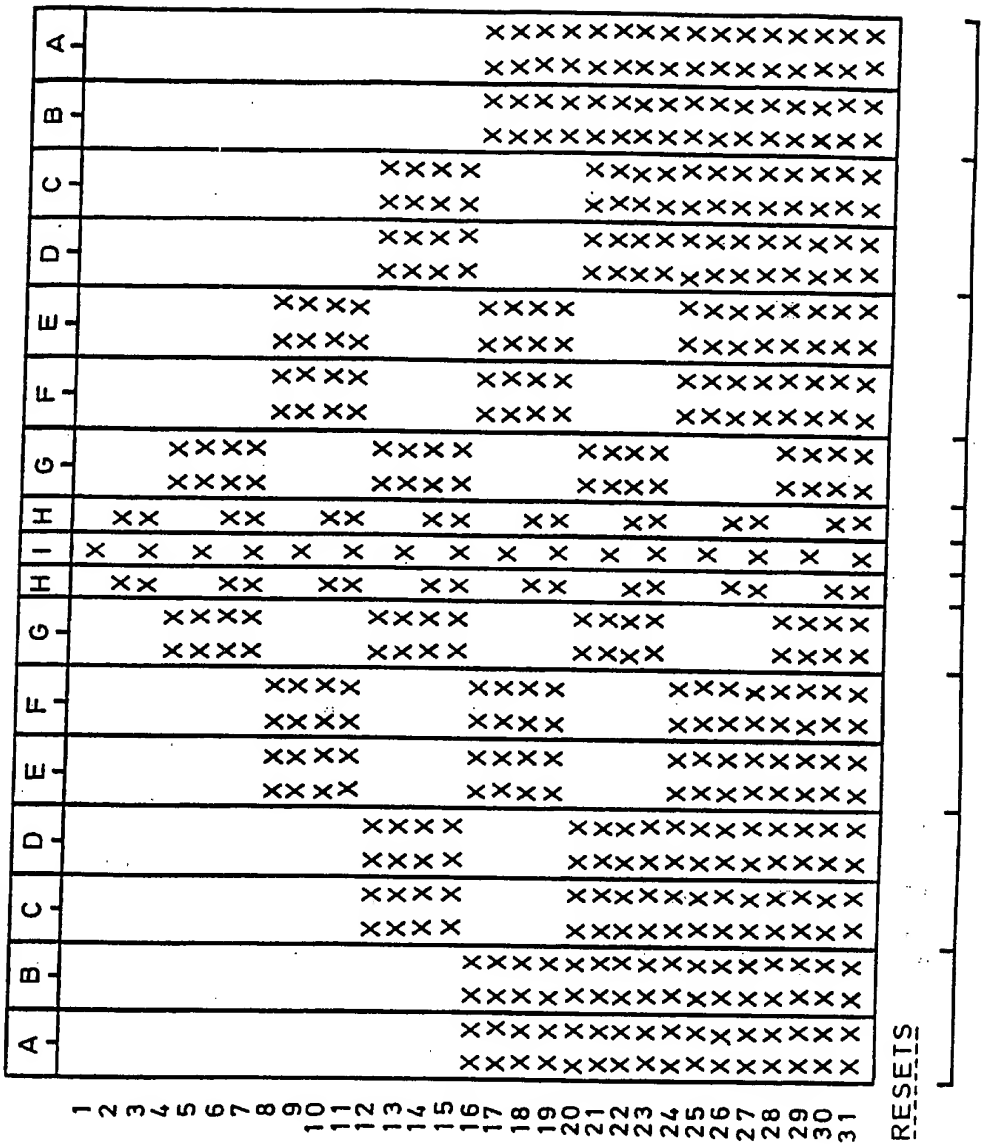
RESETS

FIG.12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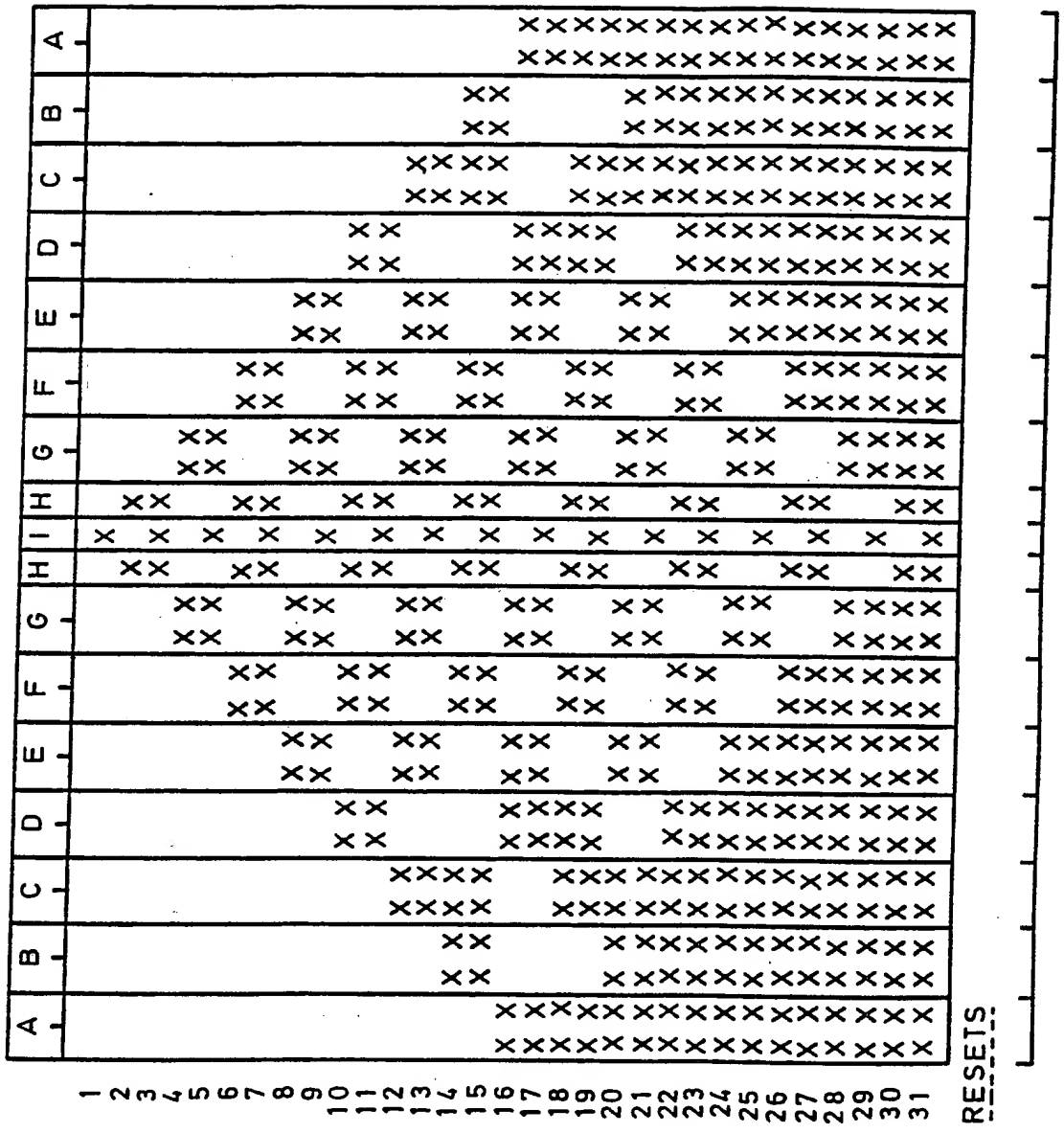
RESETS

FIG.11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RESETS

FIG.13

FIG. 14

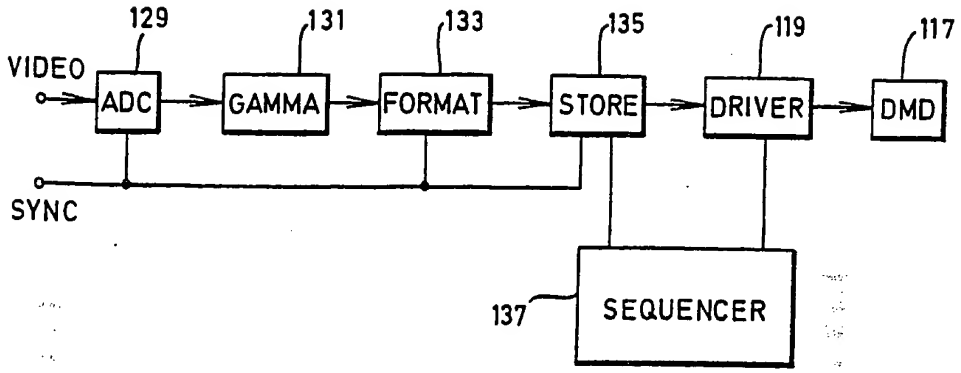


FIG. 15

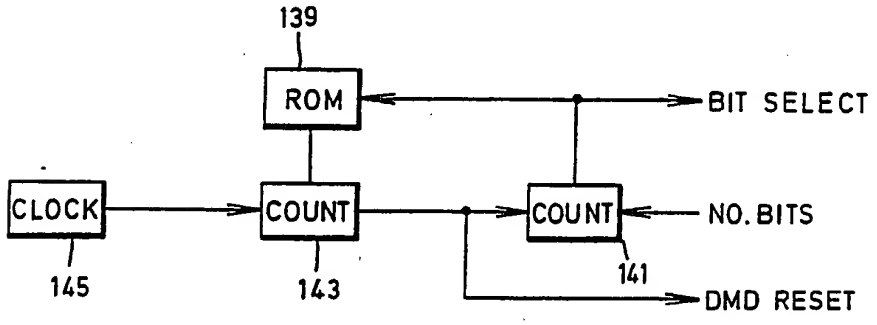
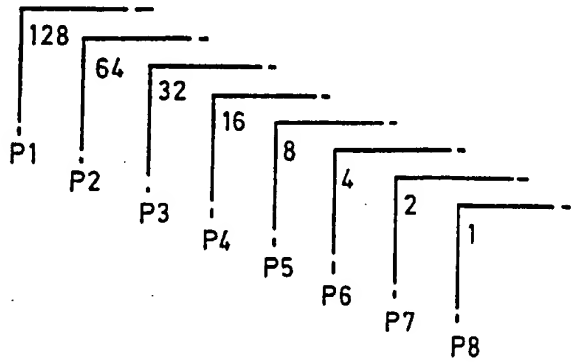


FIG. 16



INT. NATIONAL SEARCH REPORT

International Application No
PCT/GB 93/02129

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 G09G3/34 H04N3/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 G09G H04N G02B G09F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO,A,92 12506 (RANK BRIMAR LTD.) 23 July 1992 cited in the application see Abstract see page 13, line 4 - page 14, line 22; figures 1,2,4,7,8 see page 23, line 1 - page 24, line 4	1-5,9, 10,14-16
Y A	WO,A,90 12388 (CIRRUS LOGIC INC.) 18 October 1990 see Abstract see page 31, line 9 - page 32, line 7; figures 7B,8	1-5,9, 10,14-16 6

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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Date of the actual completion of the international search	Date of mailing of the international search report
10 February 1994	25.02.94

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Corsi, F

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International Application No
PCT/GB 93/02129

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP,A,0 261 901 (THORN EMI PLC) 30 March 1988 see Abstract see page 4, line 30 - page 5, line 26; figures 1,4,7-10	4,5
A	EP,A,0 261 896 (THORN EMI PLC) 30 March 1988 see Abstract see column 4, line 43 - column 5, line 47; figures 1-3	12
A	WO,A,92 09064 (RANK BRIMAR LTD.) 29 May 1992 see Abstract see page 12, line 9 - line 36; figures 8-10,14	1,10,11, 14

IN RNATIONAL SEARCH REPORT

Information on patent family members

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PCT/GB 93/02129

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		EP-A-	0466835	22-01-92
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